

AUDIO MONITORING AND CONVERSION

APPARATUS AND METHOD

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BACKGROUND OF THE INVENTION

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1. FIELD OF THE INVENTION

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The invention relates to the utilization of electronic signals, and finds particular usefulness with audio signals, in digital and/or analog forms, such that the audio signals may be operated on to obtain programs of particular audio information or characteristics. While the invention pertains generally to any manipulation of an electronic type signal and especially audio and audio type signals, it will find particular utilization in the film and television industries where the audio portion of entertainment or educational programs is manipulated in order to create, edit and/or distribute (broadcast) such programs.

The present invention relates to the field of manipulation of electronic signals, and finds particular usefulness in manipulation of audio signals for program applications. The preferred embodiment of the invention is described herein with respect to audio type signals by way of example to those of ordinary skill in the art. The preferred embodiment given by way of example pertains in particular to cost effective and operator convenient apparatus and method for monitoring television and film program audio signals, combined with the ability of converting the audio signals from analog to digital or digital to analog forms, converting digital sample rates and providing testing, monitoring and manipulation of analog and digital forms of the signal(s) as well

1 as providing mixing of audio signals, commonly referred to in the industry as voice over.

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2. DESCRIPTION OF RELATED PRIOR ART

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The invention will be described by way of example in respect to its preferred embodiment as

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used in the television and film industries. In television and film production and distribution

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facilities it is common to perform various monitoring and processing of audio signals, with each

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instrument used providing one or two of the following functions: visually monitoring, audibly

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monitoring, converting analog to digital, converting digital to analog, converting sample rate,

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locking sample rate to a reference, monitoring for digital errors, controlling level, mixing signals,

10 inverting polarity, reversing and/or redirecting channels, and testing audio signal equipment. It is

11 common for a television or film production facility to have numerous pieces of equipment which

12 together can, if suitably enabled by one or more skilled operators, provide any of all of the above

13 functions and capabilities. Unfortunately this equipment is expensive and complex, placing its use

14 out of the reach of the relatively unskilled operator, and placing the cost out of the reach of the

15 relatively budget constrained facility. In particular, in many low and medium budget television

16 stations and production facilities, money has not been available to acquire the equipment and train

17 the operators to perform all of the desired manipulation, monitoring and processing functions and

18 capabilities, including those mentioned above. Fortunately these facilities have heretofore been

19 able to operate utilizing relatively unsophisticated and limited equipment in conjunction with

20 analog audio signals, foregoing the desired capability to perform various ones, many or all of the

21 above mentioned functions.

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With the transition to digital broadcasting and in particular to high definition digital

1 broadcasting with accompanying high quality and multiple channels of digital audio, which
2 operation has been mandated by Congress, many small and medium budget facilities can not
3 afford to purchase the many individual pieces of equipment, hire the skilled operators and provide
4 the operator training needed to convert their existing analog signals and equipment for use in the
5 mandated high quality digital broadcasting. There is as a consequence a great need for (relatively)
6 low cost apparatus and methods which can incorporate many or all of the above desired features
7 and be operated by relatively lower paid and relatively unskilled operators.

8 The present invention overcomes the above described and other prior art cost and operator
9 disadvantages by providing the capability of performing many of the most needed audio signal
10 manipulation, monitoring and processing functions and capabilities in an inexpensive, simple and
11 easy to use fashion which may be utilized by relatively unskilled operators in low and medium
12 budget facilities. It is expected that the low cost and convenience afforded by the herein described
13 inventive features will be appreciated and used by facilities of all sizes as it is made available and
14 known thereto by the teachings herein.

16 BRIEF SUMMARY OF THE INVENTION

17 The present invention provides a cost effective and simple to operate capability of
18 manipulating, monitoring and processing analog and/or digital signals, and is especially applicable
19 to audio signals, to provide visual monitoring, audible monitoring, conversion from analog to
20 digital and digital to analog, converting sample rate, locking sample rate to a reference, monitoring
21 for digital errors, controlling level, mixing signals, inverting polarity, reversing and/or redirecting
22 channels, and testing audio signal equipment. Monitoring as described above may refer to

1 monitoring of levels, monitoring of frequency content (for example energy content or amplitude or
2 response at various frequencies), monitoring of distortion, monitoring of errors, or any other
3 monitoring which is useful in producing or distributing electronic signals and particularly audio
4 signals.

5 A low cost apparatus embodying the invention is described herein by way of example with
6 respect to the preferred embodiment, which apparatus makes use of several novel signal
7 processing, interconnection, sharing and other techniques which provide a high degree of
8 flexibility and performance as well as ease of use, at a low cost.

9 Of particular novelty is the combination of the mixer with one or more of the above features
10 which may be utilized as a voice over feature with digital audio signals, for example the
11 combination of a visual level monitor and voice over mixer and visual level monitor and analog to
12 digital converter. .

13 BRIEF DESCRIPTION OF THE DRAWINGS

14 Figure 1 shows a block diagram of the preferred embodiment of the invention

15 Figure 2 shows a block diagram of the tone generator portion of the preferred embodiment
16 of the invention.

17 Figure 3 shows a block diagram of the 2 channel Audio Dissolver / Mixer portion of the
18 preferred embodiment of the invention.

19 Figures 4-8 show sheets 1-5 respectively of the preferred embodiment of the invention.

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21 DETAILED DESCRIPTION OF THE INVENTION

22 One of ordinary skill in the art will be able to practice the invention, tailored to a form

1 suitable for particular application with a particular type of signal(s) as desired, from the
2 description given in respect to Figures, taken in conjunction with the teachings set out herein. The
3 Figures show preferred and readily available industry components which are identified by industry
4 standard part number which will be recognized by one of ordinary skill who will also know to
5 substitute other components for those shown with respect to the preferred embodiment from the
6 teachings herein. In particular it is intended that the teachings herein will enable the person of
7 ordinary skill in the art to practice the inventive features with components and circuit elements
8 which are presently known, as well as with those components and circuit elements which are not
9 presently known but which will become known to the person of ordinary skill as future technology
10 developments permit.

11 Figures show significant elements of the preferred embodiment of the invention, along with
12 their significant interconnection and cooperation, for the purpose of illustrating the instant
13 invention. It will be appreciated that some minor details of elements, their interconnection and
14 cooperation are left out of the Figures for clarity and/or to avoid unnecessary recitation of what is
15 already known in the art, and one of ordinary skill in the art will nevertheless know to practice the
16 invention from the teachings herein without resorting to undue experimentation or further
17 invention. In particular, single lines are shown with arrows indicating primary level
18 interconnections to elements shown as boxes. One of ordinary skill in the art will know that many
19 of these lines represent multiple connections with multiple signals which flow both in the main
20 directions given by the arrows, but also in reverse direction as is common in the art. Additionally
21 one of ordinary skill will recognize that the boxes showing various elements represent known
22 circuitry constructed of known electronic components, with various internal interconnections,

1 again not shown for clarity. Despite the abbreviations to the drawings which are made for purposes
2 of clarity and/or avoiding unnecessary complexity, the person of ordinary skill in the art will know
3 from the present teachings to practice the invention, including the details of construction which
4 have been omitted.

5 **Figure 1** shows a block diagram of the preferred embodiment of the invention which is
6 given by way of example. Remote (for example computer) control connections 1 and 2 are
7 provided in well known RS232 form which in conjunction with RS-232 buffer 3 provide remote
8 control of the invention through connection with Z8 microprocessor 4. Other forms of remote or
9 computer control, as well as other types of processors 4 may be practiced as will be known to one
10 of ordinary skill from these teachings. The microprocessor operates to configure and control the
11 various programmable components utilized throughout Figure 1, as well as providing various other
12 computer operations via its bus management unit 7, both operating with respective control, address
13 and data interconnections, as will be described more fully below. Microprocessor 4 operates with
14 a program and data storage, which is preferred to be electrically erasable read only memory, EE-
15 ROM 5, which holds the operating program for 4 as well as various data and configuration
16 information relating to the operation of the invention. As one example, various operating
17 parameters set by the human operator, such as input signal selection, volume level, output signal
18 frequency reference and others may be written into a section of 5 by processor 4 and stored so that
19 in the event of a power failure all of the stored operating parameters may be safely preserved,
20 allowing processor 4 to return the operation to the condition existing before the power failure upon
21 the return of power. This is a very useful feature in that no operator intervention is required to
22 place everything back into operating condition after an absence of power. Other memory and

1 processor configurations may be utilized as well as will be known from the teachings herein.

2 Microprocessor 4 also communicates with a 2 line display 6 for displaying messages to the
3 operator or others. This display contains internal memory which stores the displayed message and
4 4 may read from or written to this memory. Other display configurations may be utilized as well as
5 will be known to one of ordinary skill. Additionally, data which is stored in update E-Rom 9 may
6 be accessed via Bmu 7 (buss management unit) and utilized to configure various components, for
7 example the optional Tone Generator and Mixer of 8 and Sample Rate Converter 13.

8 Various audio inputs which take on various forms may be utilized with the present
9 invention. In particular the preferred embodiment may receive well known professional digital
10 AES/EBU data stream 14, consumer S/PID (a.k.a. S/PDIF) data stream 15, SMPTE data stream 16
11 or analog signal 21. These input signals may be present with standard sample rates, for example
12 32, 44.1, 48 or 96 kHz, or may have nonstandard sample rates. It is preferred to utilize a digital
13 receiver 13 which accommodates a wide range of sample rates, for example the Crystal
14 Semiconductor CS8420-CS. If desired, an optical interface may be utilized to receive an input
15 signal in one or more of the known optical (for example fiber optic) interfaces.

16 Field Programmable Gate Array, FPGA 8 provides optional Tone Generator and Audio
17 Mixer in conjunction with optional E-Rom 10 and Flash Rom 11 as will be described in more
18 detail with respect to Figures 2 and 3. FPGA 8 also provides clock, timing and control signals for
19 various of the audio signal processing operations such as sample rate conversion and digital audio
20 receive and transmit. In particular, FPGA 8 operates to receive television sync (i.e. video sync
21 from a video signal) 17 and in conjunction with VCO 19 and LPF 20 operates as a PLL to phase
22 lock various signals such as the digital audio sample clock to the television sync. In this manner,

1 digital audio may be frequency and/or phase synchronized to the video to facilitate handling of
2 related audio and video signals within television or film systems. This feature is of particular use
3 whenever digital audio and video (or film) must be combined into a single data stream (or on a
4 film) such that a fixed and known number of audio samples are combined with a fixed and known
5 number of video samples or frames. This practice prevents the problem of missing or duplicated
6 audio samples from occurring in the combined data stream (or on the film) which in turn prevents
7 clicks and pops from occurring in the audio program. Alternatively, 8 also provides (under control
8 of 4) clock, timing and control signals for various of the audio signal processing operations which
9 are locked to the incoming digital signal sample rate, or to a fixed crystal frequency from 18. In
10 this fashion (and assuming the presence of Sample Rate Converter option of 13) the output digital
11 signal sample rate may be locked to the input sample rate, locked to video 17 or a fixed frequency
12 which is crystal derived. It is preferred that differing standard frequencies may be selected which
13 may then be referenced to the selected reference all under control of the microprocessor 4 in
14 response to an operator set priority or scheme as will be described further herein. For example,
15 standard frequencies of 32, 44.1, 48 and 96 kHz may be selected for the output signal, with the
16 selected frequency being referenced to video 17, crystal oscillator 18 or one of the input signals
17 14, 15 or 16. Of course, by the simple addition of another receiver 13 and if desired a mux 12, it
18 will be possible to lock the output signal from a given input, for example 14 to another input, for
19 example 16. It will also be possible to provide the same audio signal in differing output sample
20 rates by utilizing multiple output drivers 26 as will be described in more detail below.

21 It will be recognized that each or any of these input signals may carry multiple audio signals,
22 examples including two channel stereo, four channels for example consisting of four surround

1 channels or two stereo channels in two languages or 5.1 channel Dolby™ surround sound. The
2 preferred embodiment described herein utilizes two channel stereo, but one of ordinary skill in the
3 art will know to utilize the invention with any desired number of signals from the present
4 teachings.

5 Digital inputs 14, 15 and 16 are coupled to an input multiplexer 12 where, under control of
6 the processor 4, the desired input signal is selected. The selection of input signal may be
7 automatic, with the processor 4 receiving information from 13 as to whether or not a particular
8 input has a signal present, and if not moving to the next input. The sequence and ones of tested
9 inputs may be programmed in manufacture, but is preferred to be selected by the operator. For
10 example 4 may be programmed to look at 14 first to see if a signal is present, and if not to look to
11 another input but if there is a signal present to remain on 14 until such time as the signal is no
12 longer detected, at which time it looks at 16 to see if a signal is present, and if so to remain there
13 until no signal is detected, at which time it looks at 15. Alternatively, 4 may be programmed to
14 only look to 16 and if no signal is present to look to 14, and if no signal is present to look again to
15 16, with the inspection of 14 and 16 continuing at predetermined intervals until a signal is found.
16 With the capability of 4, the user may configure the automatic inspection and selection of inputs
17 based on particular criteria which is important to the user's system. As another example, 4 may be
18 configured by the user to look to 16, and if it is not present, for a user programmed period of time
19 to switch to 14 for a predetermined amount of time, during which a message such as "audio
20 problems are being experienced by the network" is played back by a recording device (triggered
21 by 4 via 2) after which input 16 is again selected. This automatic playback of messages may be set
22 to continue for the duration of the absence of 16. From the teachings herein one of ordinary skill in

1 the art will know to utilize different variations of such automatic operations feature of the
2 invention to suit particular applications.

3 One of ordinary skill in the art will recognize that in the present description which deals with
4 the absence of a signal, that such description may apply as well to a signal which is present but
5 which exhibits one or more significant error(s). The automatic or programmed operation may very
6 well take into account such factors as the number and type of errors present, and the time and/or
7 frequency of their presence in making a determination to switch from one input to another, or to
8 remain on a known input. The selection of inputs may include analog, digital or optical inputs as
9 desired.

10 The above description of automatically selecting an input for purposes of selecting an audio
11 signal will also be useful for selecting an input for use as the frequency reference for the internal
12 clocking and/or output signal clock rate as well. The selection of the particular input(s) to be used
13 as a reference (as compared to that used for the program audio signal) may follow the same control
14 as the program audio selection or may follow different related or independent control. Again such
15 factors as signal presence, type of errors present, and the time and/or frequency of their presence
16 will be useful factors which may be programmed in manufacture, or selected by the operator, in
17 making a determination to switch from one input to another, or to remain on a known input for use
18 as the reference. The selection of inputs may include analog, digital or optical inputs as desired.

19 The digital input is received by Digital Audio Rx 13 which optionally includes a sample rate
20 converter. Receiver 13 performs equalization, clock recovery, digital data stream characterization
21 and error checking of the selected audio input, and provides the recovered clock, data stream
22 characteristics, audio data and error data to the other circuitry. The data stream characterization

1 and error checking allows the nature of and defects in the digital data to be determined and
2 reported to the processor 4 for possible action.

3 The novel configuration of selecting the desired digital audio signal is achieved by the
4 nonobvious use of an analog signal multiplexer 12 to couple the desired digital signal 14, 15 or 16
5 to the Receiver 13. In this fashion the cost of having a separate digital receiver for each digital
6 input, followed by a digital selector, is avoided.

7 The optional sample rate conversion of 13 may be utilized to provide digital output signals
8 at a sample rate slightly or greatly different from the input signal, for example a 44.1 kHz sample
9 rate signal from the S/PID input may be converted to 48 kHz which is phase locked to video as
10 provided by 8. The control of the Sample Rate Converter may be automatic, with 13 identifying
11 the sample rate of the incoming digital signal to the processor 4, which in turn configures 13 to
12 convert the incoming rate to a desired rate which has been previously selected. This operation may
13 be programmed either in manufacture or by the operator. Additionally the Sample Rate Converter
14 allows the receiver to capture digital data streams which are off frequency due to defects in the
15 transmitting equipment. For example satellite or internet transmission of digital data streams can
16 impart unwanted frequency shifts and/or phase jitter to the sample rate of the data stream, which
17 may be corrected by the Sample Rate Converter to provide an output sample rate which is
18 frequency locked to stable internal crystal 18. The selection of an output sample rate which is not
19 locked to the incoming sample rate is preferred to be automatic, occurring under control of
20 processor 4 whenever receiver 13 reports frequency variation or other errors above a
21 predetermined level which is set in manufacture or by operator.

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1 Also shown in Figure 1 is an analog audio input 21 which is buffered by 22, gain adjusted
2 by 23 to achieve volume (or level) control, buffered again by 24 and converted to digital at the
3 desired sample rate by 25. The sample rate is selected by 4 via 8 as described elsewhere herein.

4 The digital audio data and corresponding clock and control signals from 25 and 13 are
5 coupled to FPGA 8. Processor 4 makes a selection of one or the other audio signal from 13 and 25,
6 or both, to be utilized. Audio from 13 or 25 may simply be selected by 4 to be output, or they may
7 be mixed together in 8 (under control of 4) or may be delayed, or multiple of these operations may
8 be performed as is be described herein. The selected (or mixed or delayed) digital audio is then
9 coupled via 29 for conversion to analog by 30-38, and to 26 for outputting as one or more digital
10 signals.

11 Element 26 is a standard digital audio transmitter circuit, a Crystal Semiconductor CS8420-
12 CS which processes the input digital audio signal to provide industry standard AES/EBU and
13 SMPTE digital audio signals. Recall that the sample rate which is utilized by 26 for these signals
14 may be of a particular frequency and referenced to a particular source under control of 4. Multiple
15 elements 26 operating in parallel, or separately, may be provided is desired to provide multiple
16 output signals with differing characteristics. For example multiple outputs each having a different
17 sample rate and/or different delay may be provided.

18 Digital audio from 13 or 25 (or mixed from 8) is coupled to 29 and the selected one is
19 displayed on visual Bar Graph Display 33. It is preferred that this display consist of 64 LEDs, 32
20 for each channel and displaying in substantially 3 dB increments the instantaneous and average
21 levels of the audio signal in each channel as is well known in the art. Other types of visual displays
22 will be known suitable for this function as well.

1 Digital audio from 29 is also coupled to a precision D/A converter 30 where it is converted
2 to analog, which is coupled via buffer amplifier 31 to analog line output 32. Buffer 31 is preferred
3 to include level setting jumpers or other adjustments to enable the operator to set the analog output
4 level of 32 to a desired value. The elements 30 and 31 are preferred to be options as not all
5 systems will have need of an analog line output. Multiple buffers 31, coupled to D/A 30 may be
6 provided if desired, and multiple D/As 30 may also be provided in additional line outputs are
7 desired.

8 Digital audio from 29 is additionally coupled to a monitor D/A converter 34 where it is
9 converted to analog, which is coupled via Power Amp 38 to analog line outputs 39 and 40. Output
10 39 is preferred to be connected to speakers which are internal to the housing of the device utilizing
11 the invention whereas output 40 is preferred to be a standard plug and socket type connection for
12 use with headphones. Buffer 38 is preferred to include a level setting adjustment to enable the
13 operator to set the output level of 39 and 40 to a desired value. Analog audio from 34 is coupled
14 via volume control 35 and Power Amp 36 to output 37 which is preferred to be connected to
15 external speakers. With the above configuration the operator may choose to audibly monitor the
16 audio signal(s) by use of headphones, internal speakers or external speakers.

17 While various output forms of the processed audio signal are shown by way of example,
18 such as 27, 28, 32, 37, 39 and 40 one of skill in the art will know from the teachings herein that
19 such output signals may be removed, duplicated or multiplexed as needed to fit or satisfy a
20 particular system or other needs as desired. For example, the digital output signals 27 and 28 may
21 be combined into one output which is optionally configured to AES/EBU or SMPTE format. As
22 another example signals 32, 37, 39 and 40 may be combined in one output which is configured to

1 fit the particular application. The configuration may be by manufacture, operator or automatic. For
2 example, an analog output may automatically configure to appropriate output level and power by
3 sensing the load impedance which is connected. A low impedance, for example 8 Ω , would cause
4 the output to be configured to drive a speaker by including volume control 35 and power amplifier
5 36. A higher impedance, for example 600 Ω , would cause the output to be configured to drive at
6 line levels by including buffer amplifier 31. An even higher impedance, for example 2000 Ω ,
7 would cause the output to be configured to drive a headphone by including volume control 35 and
8 power amplifier 38. Similarly, if the output sensed a load of 75 Ω it would be configured as a
9 SMPTE digital output, and if it sensed a load of 150 Ω it would be configured as an AES/EBU
10 output. A particularly cost effective arrangement may be utilized having one or more digital
11 outputs which automatically configure as SMPTE or AES/EBU and one or more analog outputs
12 which automatically configure as speaker, line or headphone outputs.

13 One of ordinary skill will recognize from these teachings that ones or all of the elements 26
14 through 40 may be eliminated or provided in duplicate if desired, in order to reduce cost or to
15 provide audible or visual monitoring of multiple programs or with multiple types of monitors
16 and/or outputs in order to fit a particular system or requirements.

17 It has been above suggested to delay the audio signal as part of the operation of the invention
18 and in particular it is suggested to be part of the signal processing which takes place. Such delay is
19 often useful in maintaining audio to video timing or lip sync, in systems where significant amounts
20 of video delay are present due to video signal processing. Such delay may be added at virtually
21 any point in the signal path, however it is preferred to occur in conjunction with and as part of the
22 sample rate conversion 13, as is taught in detail in U.S. patents 5,920,842 and 6,098,046. The

1 combination of variable delay and sample rate conversion elements makes the inclusion of pitch
2 correction to allow rapid delay changes without pitch errors is highly desired. Control of the
3 amount of delay, pitch correction, pitch shifting (with or without delay change) and other delay
4 related functions may be automatic, programmed or via remote control all as taught in the
5 aforementioned patents. In particular, the addition of an input for a video processor's digital delay
6 output signal (DDO) will find considerable use in many applications. This signal is used to convey
7 the amount of video delay to the delay portion of the device in order that the audio delay may be
8 made to match the video delay.

9 Element 41 of Figure 1 shows a switching power supply which provides necessary circuit
10 power to the various circuit elements and is preferred to utilize a wall mounted power supply,
11 commonly known as a wall wart. Other types of power supply will be known to one of ordinary
12 skill in the art.

13
14 **Figures 2 and 3** show novel details of the Tone Generator and 2 Channel Stereo Audio
15 Dissolver / Mixer respectively which are preferred to be implemented with the 10K20 FPGA 8 of
16 Figure 1.

17
18 **Figure 2** shows a novel Tone Generator which may be utilized for generating various types
19 of test signals which may be selected to be output. Figure 2 shown interconnection between ROM
20 and processor 4 via Address/Data 42. ROM is shown as E-Rom 10 and/or Flash Rom 11 of Figure
21 1. Data used for tone and test signal generation is stored in this ROM and if Flash Rom is used,
22 such data may be written into the ROM under control of processor 4, or alternatively in

1 manufacture. Data 42 in ROM is addressed from 45 via Rom Address Data 54. Rom Addresses
2 from processor 4 are latched by 44 and coupled to Rom Address Mux 45 which supplies address
3 data 54 to the ROM. For each address, the ROM returns data 42 which is coupled to either 53, or
4 via 49 to 46, 50 or 52.

5 For a particular test signal, data for only one characteristic cycle is stored in ROM. For
6 example, a sine wave at a 1 kHz frequency would have 48 distinct data values for a 48 kHz clock
7 frequency. These 48 values would be stored starting at a particular address in ROM. The processor
8 4 sends an address to 44 which selects a particular location in ROM where test signal parameters
9 such as the length of the test signal pattern (in clock cycles) and the starting address in the ROM
10 where the actual data for the pattern is located. In the previous example, the address might be 275
11 and the length 48 samples. That information is loaded (in binary) into Pattern Length latch 50 and
12 Rom Start Address latch 46, respectively. The Rom Start Address from 46 is loaded into the Rom
13 Address Counter 47 where it is then coupled via the Rom Address Mux 45 to the ROM.
14 Simultaneously with the address of the ROM data address for the selected test signal being placed
15 at 54, the Pattern Length data is loaded into Pattern Length Counter 51. As in the earlier example,
16 at the start of initialization ROM Address 54 would be the address 275 which is the start of the 1
17 kHz tone data, and 50 would contain length 48. As soon as processor 4 tells the generator to Run
18 55, the pattern length counter 51 is incremented at every clock 56, which generates a new address
19 which is coupled via 47 and 45 to become ROM Address 54. By this operation every one of the 48
20 data values for the 1 kHz tone is addressed by 54 with that data appearing at 42 to be loaded into
21 Audio Data Shift Register 53 which outputs serial data which is selected by 8 to be coupled to 26
22 and/or 29 for utilization by the system.

1 One of ordinary skill in the art will recognize that for a sign wave, it is actually only
2 necessary to store values for 1/4 of a total sine period, these being the unique values to the sine
3 wave. Thus for the 48 sample example above, only 12 unique samples may be stored, and by
4 utilization of inversion and reversal all of the 48 values for the entire period may be had. This
5 reduction in storage to the truly unique values may be had for many different test signals, allowing
6 conservation of memory as well as improved performance, and may be practiced as desired in the
7 practice of the inventive features described herein. The conversion of the stored unique values to
8 the entire waveform period of values may be performed by dedicated circuitry as part of the
9 address and data elements 44-47 and 50, 51, or may be performed by the microprocessor 4, or a
10 combination of the two as will be known to one of ordinary skill in the art from the teachings
11 herein.

12 Elements 48 and 49 allow the microprocessor 4 to send and access data and address
13 information from one bus via the other, 52 allows the processor 4 to load control signals into a
14 register for storage, for example to load the run signal 57 which instructs the counters 47 and 51 to
15 run and Mux 45 to change to the run state. Register 52 thus turns tone generator on/off via run
16 signal. Other control functions may be stored in 52 as well and utilized to provide other control
17 signals (not shown). These inventive features allow flexibility and reduced cost by permitting the
18 microprocessor 4 to interact more efficiently with other devices which are connected to the data
19 and address busses 42 and 43.

20

21 **Figure 3** shows a novel 2Channel Stereo Audio Dissolver / Mixer feature of the preferred
22 embodiment. Note that only one channel each of Program Audio and Voiceover Audio are shown

1 for clarity. The preferred embodiment utilizes stereo channels, and one of ordinary skill in the art
2 will recognize that both left and right channel operation is desired, which is preferred to be
3 achieved by operating at double the single channel speed. From the teachings herein, one of
4 ordinary skill will be able to utilize these inventive features with 5.1 channel audio, or any other
5 number of channels for program audio or Voiceover audio or both, as desired.

6 Program Digital Audio data 60 from 13 is latched into 62 and passed to 36 bit Holding &
7 Shift Register 64. Similarly, Voiceover Digital Audio data 61 from 25 is latched into 63 and
8 passed to Holding & Shift Register 65. The remainder of the circuit of Figure 3 operates to mix the
9 signals 60 and 61 by dissolve factors α and $1-\alpha$ respectively, where α ranges from 1 to 0. The
10 dissolve factor can be thought of as the coefficient which is multiplied with the signal to achieve
11 fading or gain control. Thus if the signal is multiplied by 1 it is passed at full amplitude, if
12 multiplied by .5 it is passed at half amplitude, and if multiplied by 0 is is not passed. As α
13 changes from 1 to 0, the effect is to fade Program Audio 60 down while at the same time fading
14 Voiceover Audio 61 up. This is a useful effect which allows an operator to fade program audio
15 down by several dB (or even to inaudible or zero levels) while simultaneously fading an
16 announcer's voice up so that the announcer's message is mixed with the program audio for the
17 period of time of the announcement. The unique circuit may also be utilized simply for gain
18 control or other multiply type functions on any of the signals.

19 The particular apparatus and method of the Audio Dissolver / Mixer is novel, being highly
20 efficient, high performance and low cost. This Audio Dissolver / Mixer apparatus and method will
21 find use in many applications other than the instant invention, for example such as implementing
22 multiplier/accumulator cells for generalized signal processing and filter uses. For explanation, it

1 will be assumed by way of example that audio samples are latched into 62 and 63 at 48 kHz rate,
2 that is at every 48 kHz clock new data is loaded into 62 and simultaneously into 63. The elements
3 64-66 & 68-70 operate at 64 times that 48 kHz clock rate. The Dissolver / Mixer operation of 64-
4 70 operates in ping/pong fashion such that a bit of data from 64 is selectively accumulated in 70
5 (with appropriate weighting) according to a bit of α from 67, followed by a bit of data from 65
6 being selectively accumulated in 70 (along with the immediately prior accumulated value)
7 according to a bit of $(1-\alpha)$ from 67, followed by the next bit from 64, and then the next bit from
8 65, etc. until all 24 bits of each data byte which was latched into 62 and 63 is operated on. It may
9 be noted that the action of 64-66 & 70 operates at 64 times the 48 kHz clock and thus would be
10 capable of operating on 32 bit bytes in 62 and 63, however for convenience the preferred
11 embodiment uses only 24 bit bytes from 62 and 63, which are shifted in special fashion into 62
12 and 64 with the remaining 8 bits capability for each byte simply being unused.

13 To initialize the operation at every 48 kHz clock cycle three bytes of data for a Program
14 Audio sample, Voiceover Audio sample and mix coefficient α are simultaneously loaded into
15 registers 62, 63 and 67, respectively. At the same time, the value in accumulator 70 is cleared to 0.

16 At the start of this 64 X 48 kHz clock cycle (i.e. 1 - 48 kHz clock cycle) audio data from the
17 two channels 62 and 63, is shifted in special fashion into the output of 64 and 65 to provide the 24
18 bits of each audio sample data in 62 and 63 in 36 bit form. The special shift involves shifting each
19 24 bit word by 12 bits toward the LSB, thus dividing by 2^{12} , and padding the 12 most
20 significant bit positions in the register 64 and 65 with the sign bit. This action loads the audio
21 sample into the Holding & Shift Register as a 36 bit value which is the audio sample divided by
22 4096, while maintaining full precision of the original 24 bit sample value.

1 Multiplexer 66 first selects the Program Audio, to be applied to adder 69. At the same time
 2 the LSB of the coefficient α which is stored in 67 is shifted to the output of 68 and applied to
 3 accumulator 70. In the instance where the bit applied to 70 from 68 is low, the accumulation is
 4 inhibited, thus holding the previous value in 70 until the next cycle. If the bit from 68 is high, the
 5 accumulator is enabled to add the value from 64 to the accumulated value (which for the LSB of
 6 68 will be zero since that is the starting value of 70). Thus for the time period when the LSB of 68
 7 is selected, if the LSB from 68 is 1 the value in 64 (which is the program sample value divided by
 8 4096) will be stored in 70. If the LSB from 68 is 0, the existing 0 in 70 is maintained unaltered.

9 After the LSB from 68 and the sample from 64 are operated on, the sample from 65 is
 10 operated on. This sample is the Voiceover audio value which has also been divided by 4096 as was
 11 the program audio sample. The accumulate process is repeated for the value in 65. Next, the shift
 12 registers 64, 65 and 68 shift to the next higher bit position (LSB + 1) such that the value in 64 is
 13 the program audio sample divided by 2048, 65 holds the Voiceover audio divided by 2048 and 68
 14 holds the next to LSB of the 12 bit coefficient from 67. The accumulate process is then repeated.
 15 The shift registers 64, 65 and 68 again shift to the next higher bit position (LSB + 2) and the
 16 values in 64 and 65 again accumulated according to the bit in 68. The shift and accumulate process
 17 is repeated until all 12 divided values ($\div 4096$ through $\div 2$) have been accumulated in accord with
 18 the corresponding bit of the scale factor in 67. At the end of the 48 (2 signals X 2 channels each X
 19 12 bit coefficient) clocks nothing happens for the remaining 16 clocks (2 X 8) and the accumulator
 20 value is held. At the start of the next cycle, the accumulator value is loaded into 71. This
 21 accumulator value corresponds to α times the Program Audio sample value in 62 + $(1-\alpha)$ times the
 22 Voiceover Audio sample value in 63. In other words it is a mix of the two samples, α times the

1 value in 62 plus $(1-\alpha)$ times the value in 63. At the next instant, the accumulator value is cleared to
2 zero, new audio sample values are loaded in 62 and 63, a new coefficient α is loaded into 67 and
3 the process starts anew. The output of 71 is a 48 kHz stream of mixed values 72 which is passed to
4 26 and/or 29.

5 Note that in the preferred embodiment the 24 bit audio programs are multiplied by a 12 bit
6 coefficient to perform a fade between the two. It may be recognized that many values which a
7 traditionally multiplier would be capable of accepting are never used, with the preferred
8 embodiment taking advantage of that fact in order to reduce the amount of complexity necessary
9 to perform the desired operation as compared to the traditional approach of utilizing 16x16 bit
10 multipliers. From the teachings herein, one of ordinary skill in the art will recognize that this novel
11 embodiment may be configured to achieve any desired accuracy and precision with any desired
12 number of signals and coefficients.

13 One of ordinary skill in the art will recognize from these teachings that there are several
14 variations on this operation which may be employed. For example, instead of ping/pong operation,
15 all the divided values of 62 may be accumulated in 70 followed by all of the divided values of 63.
16 Divided values may be processed MSB first, or LSB first, or even in non-sequential order starting
17 elsewhere, as long as the appropriate dividing takes place in the Holding & Shift Register, the
18 appropriate bit is selected in 68 and appropriate weighting is accommodated in the accumulation
19 process. For example, a limited number of coefficients may be utilized in 67 in recognition of the
20 human ear's relative insensitiveness to changes in levels of loud sounds. There is no need to utilize
21 full 12 bit precision of the coefficient in 67 for coefficients which are close to 1 and savings in
22 multiply and accumulate steps may be had by eliminating coefficient precision. Additionally

1 coefficients other than α and its complement may be utilized as well, for example coefficients
2 which are not precisely related such as α and β (which would require two numbers in 67) which
3 may be preferred in order to have a nonlinear mixture of the two audio signals. Of course, one of
4 ordinary skill must ensure that such problems as overflow of the accumulator or undesired loss of
5 precision do not occur when selecting a desired precision of coefficient(s) and accumulation.
6 Instead of utilizing a single bit at a time, multiple bits may be accumulated, again as long as the
7 appropriate weighting is applied.

8 Control of the dissolve from program audio to voice over audio (by coefficient of α) may be
9 under operator control, for example by repeatedly pushing a button which causes a change of some
10 amount, for example .05, for every push, or by holding the button, or in preferred form by
11 automatic control wherein 4 automatically adjusts the value of α to achieve a smooth transition
12 from Program Audio to Voiceover Audio over a preselected amount of time. The start of the
13 dissolve is preferred to be controlled by a simple push of a remotely mounted or front panel button
14 and the end of the dissolve by a second push of the same button. For example, the operator
15 wishing to initiate a Voiceover announcement would push the starting button, at which time
16 processor 4 will fade the program down and the announcer up over a period of a few seconds, the
17 announcer makes the announcement after which the operator again pushes the starting button (or
18 alternatively a separate stop button) at which time processor 4 fades the announcer down and the
19 program back up. Another alternative is for the operator to hold the button until the desired level is
20 achieved at which time the button is released and the level is maintained. After the announcement
21 another push of the button returns the levels to normal. Another alternative is to use two buttons,
22 one for fade up and one for fade down, the operation being automatic upon a single push, or at a

1 controlled rate as the button is held. As yet another alternative, a rotary or slide type of control
2 may be included whereby the operator mechanically positions the control to achieve the desired
3 degree and speed of fade. Such may be accomplished by utilization of a digital encoder which
4 outputs a digital number representative of the degree of movement of the mechanical control as is
5 well known in the art. It may be noted that frequently the announcer will be the operator, making
6 both the announcement and controlling the operation of the audio mixer. One of ordinary skill in
7 the art will be able to configure an appropriate interface to the operator to fit a desired system and
8 method of operation from the teachings herein.

9 **Figures 4-8** are sheets 1-5 respectively of a schematic diagram showing the detailed
10 configuration of the preferred embodiment of the invention. The schematic diagram corresponds
11 directly to the overall block diagram, but provides additional detail which will aid the person of
12 ordinary skill in the art in understanding the inventive concepts discussed above.

13 Figure 4 shows U1 the Z8 microprocessor corresponding to 4 of Figure 1. Note that a
14 second, test, version of U1 is provided at TS1 for aid in troubleshooting failures. J6 of Figure 4
15 corresponds to 1 and 2 of Figure 1 and U3 to 3. U7 corresponds to 5, U4 to 7, U6 to 8. J4 is the
16 connection for 33 which is not shown.

17 Figure 5 shows J1 corresponding to 14, J2 (upper left) to 16 and J3 (upper left) to 15. U8 and
18 associated circuitry corresponds to 12, U10 and associated circuitry to 13 and 26, J2 (upper right)
19 to 28, J8 to 27. U9 and associated circuitry corresponds to 18, U2 and associated circuitry to 19
20 and 20. U11 and associated circuitry corresponds to 10 and 11.

21 Figure 6 shows U12 and associated circuitry corresponding to 22, U13 and associated
22 circuitry to 23, U14 and U15 and associated circuitry to 24 and U16 and associated circuitry to 25.

1 Figure 7 shows U17 and associated circuitry corresponding to 34, U18 and associated
2 circuitry to 38, U19 and associated circuitry to 35, U20 and U21 and associated circuitry to 36.

3 Figure 8 shows U 22 corresponding to 30 and U23 and associated circuitry corresponding to
4 31.

5 While the invention has been described above in respect to the preferred embodiment by
6 way of example, one of ordinary skill in the art will know from the teachings herein to resort to
7 various modifications, substitutions and combinations of the preferred elements and steps which
8 are taught in order to practice the invention in forms which are tailored to fit particular systems
9 and/or requirements, all without departing from the spirit and scope of the invention as claimed.

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